REMARKS

Claims 1-35 are pending. Claims 1, 6, 8, 11, 15, 18, 19, 26, 30, and 33 have been amended to recite the invention more clearly.

1. Rejections under 35 U.S.C. § 102(e) based on Robertson et al.:

Claims 1-2, 5-9, 11-12, 14-16, 18-21, 24, 26-27, 29-31, and 33-34 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,658,530 to Robertson et al. These rejections are traversed.

Claim 1 recites a circuit card including "an integrated circuit having a plurality of inputs and a plurality of outputs" and "a connector having a plurality of pins." The circuit card also includes "a plurality of conductors, each of said plurality of conductors being coupled respectively between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said pins." The plurality of conductors have "a first portion for conducting bus signals and a second portion for providing a shield." The conductors in the first portion are "grouped in a plurality of corresponding pairs, a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors."

The reference to Robertson et al. discloses a memory module in which an electrical ground pin is located between each pair of signal pins. The Robertson et al. reference does not disclose a circuit card including "a plurality of conductors, each of said plurality of conductors being *coupled* respectively between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said pins" in which the plurality of conductors has "a second portion for providing a shield." Robertson et al. also does not disclose a memory module in which the conductors in the first portion are "grouped in a plurality of corresponding pairs, a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding

pairs of said first portion of said plurality of conductors." Claim 1 and its dependent claims 2-5 are submitted as patentable over the reference to Robertson et al.

Claim 6 recites a circuit card including "a connector having a plurality of pins" and "a plurality of conductors, each of said plurality of conductors being coupled at a first end respectively to one of said plurality of pins." The circuit card also includes "an integrated circuit having a plurality of inputs and a plurality of outputs, said conductors being coupled at a second end respectively to one of said plurality of inputs or one of said plurality of outputs." The plurality of conductors has "a first portion for conducting bus signals and a second portion for providing a shield, said conductors in said first portion being grouped in a plurality of corresponding pairs." A respective one of the conductors in the second portion is "located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors."

The reference to Robertson et al. discloses a memory module having an electrical ground pin located between each pair of signal pins. The Robertson et al. reference does not disclose a circuit card with a plurality of conductors having "a first portion for conducting bus signals and a second portion for providing a shield, said conductors in said first portion being grouped in a plurality of corresponding pairs." Robertson et al. also does not teach a circuit card in which a respective one of the conductors in the second portion is "located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors." Claim 6 and dependent claim 7 are submitted as patentable over the reference to Robertson et al.

Claim 8 recites a circuit card including "a first plurality of conductive traces connecting between contact pins and an integrated circuit to conduct signals, said first plurality of conductive traces being grouped in a plurality of corresponding pairs and connected to an integrated circuit," and "a second plurality of conductive traces extending adjacent said first plurality of conductive traces to provide a shield, a respective one of said second plurality of conductive traces being located on each side of each of said plurality of

corresponding pairs of said first plurality of conductive traces, wherein said first plurality of conductive traces are part of a bus system."

The reference to Robertson et al. discloses a memory module in which an electrical ground pin is located between each pair of signal pins. Robertson et al. does not teach a circuit card with an integrated circuit and including "a second plurality of conductive traces extending adjacent said first plurality of conductive traces to provide a shield, a respective one of said second plurality of conductive traces being located on each side of each of said plurality of corresponding pairs of said first plurality of conductive traces." Claim 8 and its dependent claims 9 and 10 are submitted as patentable over the reference to Robertson et al.

Claim 11 recites a memory expansion card including "a memory device having a plurality of inputs and outputs" and "a connector having a plurality of pins." The card also includes "a plurality of traces, each of said plurality of inputs and outputs of said memory device being coupled by a respective trace to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector." The card includes "a first portion of said plurality of traces for conducting signals and a second portion of said plurality of traces for providing a shield." Traces in the first portion are "grouped in a plurality of corresponding pairs, a respective one of said traces in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of traces, wherein said first portion of said plurality of traces is part of a bus system."

The reference to Robertson et al. discloses a memory module in which an electrical ground pin is located between each pair of signal pins. Robertson et al. does not anticipate a memory expansion card having a plurality of traces which includes a "second portion of said plurality of traces for providing a shield." Claim 11 and its dependent claims 12-14 are submitted as patentable over the cited reference to Robertson et al.

Claim 15 recites a memory expansion card including "a memory device having a plurality of inputs and a plurality of outputs" and "a first plurality of conductive traces to conduct signals to said plurality of inputs or from said plurality of outputs." The first plurality of conductive traces is "grouped in a plurality of corresponding pairs." A second plurality of conductive traces is included "to provide a shield, a respective one of said second plurality of conductive traces being located to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces, wherein said first plurality of conductive traces are part of a bus system."

The reference to Robertson et al. discloses a memory module having an electrical ground pin located between pairs of signal pins. Robertson et al. does not anticipate a memory expansion card in which a second plurality of conductive traces is included "to provide a shield, a respective one of said second plurality of conductive *traces* being located to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces." Claim 15 and its dependent claims 16-17 are submitted as patentable over the cited reference to Robertson et al.

Claim 18 recites a memory expansion card including "a connector having a plurality of pins, said plurality of pins having a first portion for conducting signals and a second portion for providing a shield." Pins in said first portion are "grouped in a plurality of corresponding pairs, a respective one of said pins in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of pins." A plurality of conductive traces is "connected respectively to each of said pins, a portion of said conductive traces being connected respectively to said pins in said second portion and extending respectively along each side of conductive traces connected to said first portion of pins," and "said first portion of pins is part of a bus system."

The reference to Robertson et al. discloses a memory module in which an electrical ground pin is located between pairs of signal pins. Robertson et al. does not anticipate a memory expansion module having a plurality of pins including a "second portion for providing a shield," and a plurality of conductive traces "connected respectively

to each of said pins, a portion of said conductive traces being connected respectively to said pins in said second portion and extending respectively along each side of conductive traces connected to said first portion of pins." Claim 18 is submitted as patentable over the cited reference to Robertson et al.

Claim 19 recites a processing system including "a processing unit," and "a circuit card coupled to said processing unit." The circuit card includes "an integrated circuit having a plurality of inputs and a plurality of outputs," "a connector having a plurality of pins," and "a plurality of conductors, each of said plurality of conductors being coupled respectively between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said plurality of pins." The plurality of conductors has "a first portion for conducting signals and a second portion for providing a shield." The conductors in the first portion are "grouped in a plurality of corresponding pairs, a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors." The processing system includes "a bus system for passing signals through said processing system and said first portion of said plurality of pins are coupled to said bus system."

The reference to Robertson et al. discloses a memory module in which an electrical ground pin is located between each pair of signal pins. Robertson et al. does not anticipate a processing system including a circuit card having a plurality of conductors with conductors in a first portion "grouped in a plurality of corresponding pairs," the conductors having "a second portion for providing a shield," and "a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors." Claims 19-25 are submitted as patentable over the cited reference to Robertson et al.

Claim 26 recites a processing system including "a processing unit," and "a memory expansion card coupled to said processing unit." The memory expansion card includes "a memory device having a plurality of inputs and a plurality of outputs," "a

connector having a plurality of pins," and "a plurality of traces, each of said plurality of inputs and said plurality of outputs of said memory device being coupled by a respective trace to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector." The card includes "a first portion of said plurality of traces for conducting signals and a second portion of said plurality of traces for providing a shield, said traces in said first portion being grouped in a plurality of corresponding pairs, a respective one of said traces in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of traces." The processing system includes "a bus system for passing signals through said processing system" and "said first portion of said plurality of pins are coupled to said bus system."

The reference to Robertson et al. discloses a memory module in which an electrical ground pin is located between each pair of signal pins. Robertson et al. does not anticipate a processing system including a memory expansion card with a plurality of inputs, a plurality of outputs, and "a plurality of traces, each of said plurality of inputs and said plurality of outputs of said memory device being coupled by a respective trace to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector," wherein the card includes "a first portion of said plurality of traces for conducting signals and a second portion of said plurality of traces for providing a shield, said traces in said first portion being grouped in a plurality of corresponding pairs, a respective one of said traces in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of traces." Claim 26 and its dependent claims 27-29 are submitted as patentable over the cited reference to Robertson et al.

Claim 30 recites a processing system including "a processing unit," and "a memory expansion card coupled to said processing unit." The memory expansion card includes "a memory device having a plurality of inputs and a plurality of outputs," "a first plurality of conductive traces to conduct signals to said plurality of inputs or from said plurality of outputs, said first plurality of conductive traces being grouped in a plurality of

corresponding pairs." A second plurality of conductive traces is included "to provide a shield, a respective one of said second plurality of conductive traces being located to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces." The first plurality of conductive traces "are part of a bus system of said processing system."

The reference to Robertson et al. discloses a memory module in which an electrical ground pin is located between each pair of signal pins. Robertson et al. does not anticipate a processing system having a memory expansion card with "a first plurality of conductive traces to conduct signals" in which a second plurality of conductive traces is included "to provide a shield, a respective one of said second plurality of conductive traces being located to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces." Claim 30 and its dependent claims 31-32 are submitted as patentable over the cited reference to Robertson et al.

Claim 33 recites a method for constructing a circuit card for a bus system that includes the steps of "providing a first plurality of pins on a connector of said circuit card, said first plurality of pins for conducting bus signals," and "grouping said first plurality of pins into a plurality of corresponding pairs." The method also includes "providing a second plurality of pins on said connector of said circuit card, said second plurality of pins being connected to a respective conductive trace extending along each side of pairs of traces connected to each corresponding pair of said first plurality of pins for providing a signal shield."

The reference to Robertson et al. discloses a memory module in which an electrical ground pin is located between each pair of signal pins. Robertson et al. does not anticipate a method for constructing a circuit card which includes "providing a second plurality of pins on said connector of said circuit card, said second plurality of pins being connected to a respective conductive trace extending along each side of pairs of traces connected to each corresponding pair of said first plurality of pins for providing a signal

shield." Claim 33 and its dependent claims 34-35 are submitted as patentable over the reference to Robertson et al.

2. Rejections under 35 U.S.C. § 103(a) based on Robertson et al. and Chin et al.:

Claims 3 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of U.S. Pat. No. 6,216,205 to Chin et al. These rejections are traversed.

Claim 3 depends from claim 1, which is submitted as patentable over the reference to Robertson et al. Combining the reference to Chin et al. does not cure the deficiencies of the Robertson et al. reference. The reference to Chin et al. has been cited as providing a signal driver. Chin et al. does not teach or suggest a circuit card including "a plurality of conductors, each of said plurality of conductors being coupled respectively between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said pins" in which the plurality of conductors has "a second portion for providing a shield." Chin et al. also does not disclose a memory module in which the conductors in the first portion are "grouped in a plurality of corresponding pairs, a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors." Claim 3 is submitted as patentable over the proposed combination of the references to Robertson et al. and Chin et al.

Claim 22 depends from claim 19, which is submitted as patentable over the reference to Robertson et al. The Chin et al. reference has been cited as teaching a signal driver, and does not cure the deficiencies of Robertson et al. The reference to Chin et al. does not teach or suggest a processing system including a circuit card having a plurality of conductors with conductors in a first portion "grouped in a plurality of corresponding pairs," the conductors having "a second portion for providing a shield," and "a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors." Claim

22 is submitted as patentable over the proposed combination of the Robertson et al. and Chin et al. references.

3. Rejections under 35 U.S.C. § 103(a) based on Robertson et al. and Ortega et al.:

Claims 4, 10, 13, 17, 23, 28, 32, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of U.S. Pat. No. 6,527,587 to Ortega et al. These rejections are traversed.

Claims 4, 10, 13, 17, 23, 28, 32, and 35 depend respectively from claims 1, 8, 11, 15, 19, 26, 30, and 33, each of which is submitted as patentable over the reference to Robertson et al. The proposed combination of Ortega et al. does not cure the deficiencies of Robertson et al. Ortega et al. had been cited as teaching differential signals.

With respect to claim 4, Ortega et al. does not provide or suggest the teaching missing from Robertson et al. of a circuit card as in claim 1 including "a plurality of conductors, each of said plurality of conductors being coupled respectively between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said pins" in which the plurality of conductors has "a second portion for providing a shield." Ortega et al. also does not disclose a memory module in which the conductors in the first portion are "grouped in a plurality of corresponding pairs, a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors."

With respect to claim 10, Ortega et al. does not provide or suggest the teaching missing from Robertson et al. of a circuit card as in claim 8 with an integrated circuit and including "a second plurality of conductive traces extending adjacent said first plurality of conductive traces to provide a shield, a respective one of said second plurality of conductive traces being located on each side of each of said plurality of corresponding pairs of said first plurality of conductive traces."

With respect to claim 13, Ortega et al. does not provide or suggest the teaching missing from Robertson et al. of a memory expansion card as in claim 11 having a plurality of traces which includes a "second portion of said plurality of traces for providing a shield."

With respect to claim 17, Ortega et al. does not provide or suggest the teaching missing from Robertson et al. of a memory expansion card as in claim 15 in which "a second plurality of conductive traces" is included "to provide a shield, a respective one of said second plurality of conductive traces being located to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces."

With respect to claim 23, Ortega et al. does not provide or suggest the teaching missing from Robertson et al. of a processing system as in claim 19 including a circuit card having "a plurality of conductors" with conductors in a first portion "grouped in a plurality of corresponding pairs," the conductors having "a second portion for providing a shield," and "a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors."

With respect to claim 28, Ortega et al. does not provide or suggest the teaching missing from Robertson et al. of a processing system as in claim 26 including a memory expansion card having a plurality of inputs, a plurality of outputs, and "a plurality of traces, each of said plurality of inputs and said plurality of outputs of said memory device being coupled by a respective trace to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector," wherein the card includes "a first portion of said plurality of traces for conducting signals and a second portion of said plurality of traces for providing a shield, said traces in said first portion being grouped in a plurality of corresponding pairs, a respective one of said traces in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of traces."

With respect to claim 32, Ortega et al. does not provide or suggest the teaching missing from Robertson et al. of a processing system as in claim 30 having a memory expansion card with "a first plurality of conductive traces to conduct signals" in which a second plurality of conductive traces is included "to provide a shield, a respective one of said second plurality of conductive traces being located to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces."

With respect to claim 35, Ortega et al. does not provide or suggest the teaching missing from Robertson et al. of a method for constructing a circuit card as in claim 33 which includes "providing a second plurality of pins on said connector of said circuit card, said second plurality of pins being connected to a respective conductive trace extending along each side of pairs of traces connected to each corresponding pair of said first plurality of pins for providing a signal shield."

Claims 4, 10, 13, 17, 23, 28, 32, and 35 are submitted as patentable over the proposed combination of the references to Robertson et al. and Ortega et al.

4. Rejection under 35 U.S.C. § 103(a) based on Robertson et al. and Elabd:

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of U.S. Pat. No. 6,526,462 to Elabd. This rejection is traversed.

Claim 25 depends from claim 19, which is submitted as patentable over the reference to Robertson et al. The reference to Elabd does not cure the deficiencies of the Robertson et al. reference. Elabd has been cited as teaching implementing a processing unit and an integrated circuit on the same chip. Elabd does not combine with the reference to Robertson et al. to provide a processing system including a circuit card having a plurality of conductors with conductors in a first portion "grouped in a plurality of corresponding pairs," the conductors having "a second portion for providing a shield," and "a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of

conductors." Claim 25 is submitted as patentable over the proposed combination of the Robertson et al. and Elabd references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Peter McGee
Registration No.: 35,947
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant